REMARKS

Claim 1 stands rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 1 stands rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

The specification states that for the same voltages applied to the terminals of the NMOS pass transistor and the PMOS drive transistor the current flowing through the NMOS transistor must be greater than the current flowing through the PMOS transistor (page 5, lines 32-33 and page 6, lines 1-10). This is described in the specification as "a condition" of the memory cell. In forming the rejection under 35 U.S.C. 112 the examiner ignores the clear meaning of the condition and argues instead that the described condition occurs during circuit operation. The operation of the circuit is described starting on page 6, line 11, which states "[I]n operation .....". Rather than describing circuit operation the above-described condition simply describes what transistor current values should result if the same voltages are applied to a NMOS transistor and a PMOS transistor used to form the memory cell. The current that results when voltages are applied to the terminals of a NMOS or PMOS transistor is a function of the design and processing conditions of the transistor. Factors such as threshold voltage, gate length, and gate dielectric layer thickness can all affect the resulting current. This idea is expressed in the specification on page 6, lines 9 and 10. There it states, "[T]his condition can be achieved using well known NMOS and PMOS transistor design and processing techniques." The statement further highlights the idea that the condition for resulting transistor current refers to the NMOS and PMOS transistors individually and not to the memory cell circuit operation as suggested by the examiner.

The examiner states that there is no antecedent basis for "the same voltages" on line 21 of claim 1. Referring to page 5, lines 32-33, it is stated in the disclosure that for the same voltages applied across the gate and source/drain terminals of the NMOS and

PMOS transistors the resulting current in the NMOS transistor must be greater than the current in the PMOS transistor. There is clearly antecedent basis for "the same voltages" in claim 1.

Claim 1 stands rejected under 35 U.S.C. 102(e) as being anticipated by Leung.

In an action date 4/13/2003 the examiner states that during a read operation, the voltage applied to the word line 505 must be equal to the Vcc power supply voltage at node N1 minus the source-to-gate Vgs of the NMOS pass transistor 501 or must be less than 90% of the Vcc power supply voltage during the read operation as recited in claim 1. This statement represents a complete misunderstanding of the cited art and circuit operation in general. The voltage applied to the word line is independent of any voltage that may or may not be on N1 as well as any Vgs voltage drop. The examiner is directed to Figure 5 and the wordline 505. Any voltage can applied to word line 505. As is clear from the Figure, the applied voltage is independent of any voltage that exists in the circuit. Under the current understanding of MOS transistor circuit theory the examiners statement has little meaning. The limitation of claim 1, "during a read operation a voltage applied to the wordline is less than 90% of the supply voltage" is neither taught nor disclosed in the cited art. As such claim 1 is allowable over the cited art.

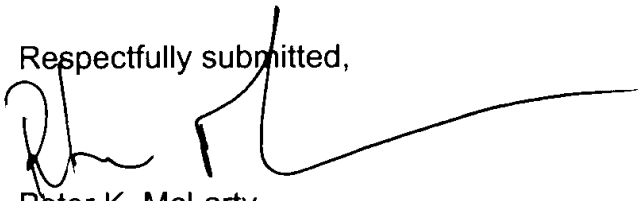
In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant amendment places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, Applicants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including

extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,



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